AIA “DESIGN FOR EXCELLENCE” WEBINAR

January 23, 2013
Learn how to:

- Minimize the risk of cost over-runs
- Reduce time to market
- Curtail sustainment costs
- Enhance product quality
- Improve overall total cost of ownership

By implementing *Design for Excellence* techniques in the design process
Design for eXcellence (DFX), as defined by Plexus

A philosophy and proven process that promotes communication and cooperation between design and manufacturing value streams responsible for the design and manufacture of end products.

What value does it bring?

- Provides continuous design process feedback
- Mitigates project cost overruns
- Improves time to market
- Enhances product performance and field reliability
- Lowers total cost of ownership
Delivering Optimized Product Realization Solutions

Conceptualize | Design | Commercialize | Manufacture | Fulfill | Sustain

THE LEADER
MID-LOW VOLUME, HIGHER COMPLEXITY
Whether as a stand-alone service or part of a collaborative development, a comprehensive Design for Excellence approach ensures a product that can be reproduced with high yields over its entire life cycle.

**Circuit Board Level**
- Design for PCB fabrication
- Design for assembly
- Design for test
  - Estimated node access
  - Enhanced node access
  - Schematic review
  - Test strategy analysis
- Design for manufacturability
  - Pre-assembly review
  - Post-assembly review
- Bill of materials analysis
  - Life cycle review
  - RoHS compliance
  - Package compatibility review

**Box Level**
- Design for high reliability
- Design for supply chain
- Design for thermal compliance
- Design for EMC
- Design for RoHS compliance
- Design for human factors
- Design for serviceability
- Design for signal integrity
- Design for box level assembly
- Design for metal fabrication
- Design for molding
PRODUCT LIFE CYCLE COST COMMITMENTS

Majority of total life cycle costs are largely determined during development.
Product development process

- Early stage – requires more ad hoc and unstructured collaboration
- Later stages – require more rigorous and structured collaboration

*Design for Excellence systems need to be integrated early and be a collaborative activity of the product development life cycle*
A & D Outsourcing Trends
The Need For A Streamlined Outsourcing Process

Jono Anderson
Principal
Engineered Products & Services
Booz & Company (N.A.) Inc.
Globally, the value proposition for outsourcing engineering design services is shifting towards more strategic drivers.

Overall Engineering Services Outsourcing Value Drivers Across Verticals

- Lower Cost: 96% (2006), 96% (2010-2020)
- Market Access: 36% (2006), 36% (2010-2020)
- Quality of Supply: 33% (2006), 33% (2010-2020)
- Government Incentives: 33% (2006), 33% (2010-2020)
- Time to Market: 17% (2006), 15% (2010-2020)
- Increasing Productivity: 6% (2006), 6% (2010-2020)
- Growing Capacity: 6% (2006), 6% (2010-2020)

Cost will be less of a driver over time.
Strategic drivers will increase in importance by 2020.

“Outsourcing of non-core capabilities for electronics is becoming the norm.” – Tier II/III Supplier

Source: Booz & Company analysis
In India, for example, aerospace engineering is expected to grow over the next 5-10 years.

source: Booz & Company analysis

The trend is to move to manufacturing globally – especially China, India, Brazil & Mexico.” – Tier II/III Supplier
Avionics, engine and power controls are amongst the first systems to have portions of design and manufacturing outsourced.

Source: Airbus A380 image from FlightGlobal, Booz & Company analysis
Focusing on avionics, engineering services outsourcing spend is projected to increase 5% per year to through 2020.

Driving Factors:
- New programs
- Retrofits
- Increasing technology complexity
- More frequent upgrades
- Safety mandates
- Obsolescence management
- Defense acquisition policies
- ATM modernization

Source: Booz & Company analysis
Avionics engineering services outsourcing will outpace most other verticals over the next decade

1) Includes avionics

Source: Booz & Company NASSCOM study, IC and analysis
Based on our survey results, of leaders in aerospace identify access to new markets and the demands on capacity as the major drivers.

### Drivers of R&D Spend in A&D

<table>
<thead>
<tr>
<th>Drivers</th>
<th>Aerospace</th>
<th>Importance by Company</th>
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<td>New Markets - Consumer Demand</td>
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<td>New Products, Segments, Capacity</td>
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<tr>
<td>New Features and Technologies</td>
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<tr>
<td>Fundamental Research</td>
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<td>Product Safety</td>
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<tr>
<td>Government Regulation</td>
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- ⬤ Most Important
- → Least Important

Source: Booz & Company analysis
Avionics have evolved quickly towards high levels of complexity making it difficult for OEMs to maintain up-to-date skillsets

Evolution of Avionics Systems & Technologies
Common Core System Architectures

**Distributed Analogue**
- Dedicated wiring
- Power supplies
- Sensor excitation
- Sensor signal voltages
- System selection & Status indications
- Dedicated LRUs / Subsystems
- Dedicated displays & controls

**Federated Digital**
- Dedicated wiring to some sensors / displays
- Digital processing used for control functions
- Software reprogrammable (off-aircraft)

**Integrated Modular Architectures**
- Use of COTS and adapted IT bus technology - 10 Mbit/sec or higher
- Use of standard modules aircraft wide installed in Cabinets/Racks pertaining to aircraft system domains
- Functionally imparted by partitioned software operating on common processors

### Characteristics
- Standard aircraft-wide dual redundant full-duplex data buses >=1Mbit/sec
- Greater use of standardized components

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Source: Civil Avionics Systems - Ian Moir, Allan Seabridge and Booz & Company Analysis

1960s - Distributed Analogue
1970s - Distributed Digital
1980s - Federated Digital
1990s & 2000s - IMA

Booz & Company
January 23, 2013

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Over the next 5-10 years, the focus of outsourcing is expected to move beyond product development and test capabilities.

### Engineering Design/Development Value Chain

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**Software**
- Req. capture
- Req. architecture
- COTS Real-time operating systems
- Embedded systems design
- High Integ. computing
- Software modeling
- Real-time code dev.
- Software traceability
- Cert. plan
- Indep. Derived Software Integration testing
- EMS services
- Software unit testing
- Software Integration testing
- Verification & validation analysis
- Fault trees
- Software Integration design
- Debugging tools

**Electrical and Electronic**
- Req. analysis and capture
- Reverse engineering
- Board layout
- FPGA des.
- Comm. protocols
- Embedded system dev.
- Embedded system dev.
- Board and Unit-level tests
- Board-level tests
- Unit-level tests
- Integ. Test
- Electronics Integration System Integration
- Obsolesc. management
- Product lifecycle mgmt.

**Other**
- Req. capture
- Req. mgmt.
- Domain expertise
- Safety analysis
- Product lifecycle mgmt.
- Config. /change mgmt.
- Product mgmt.
- QA support
- Software Verification & validation analysis
- System Integration
- Product sustain
- Obsolesc. mgmt.

Not Exhaustive
Component packaging technology trends:

- Decrease in size (length, width, thickness)
- Increase in functionality (electrical, optical, electrical mechanical and mechanical)
- Interconnection density per unit area is increasing (increased number of layers, smaller lines and spaces)
- Assembly functional performance is increasing (thermal, mechanical, electrical)

Assembly process complexities continue to increase
DFX SUMMARY

Global Environment → Conceptual Design → Initial Design → Detailed Design → Prototype Assembly

Check point

Geographical definition
- Documentation language baseline
- Date reporting
- Definition of calendar work week
- Define unit of measure
- Define numerical reporting

Material specification
- Define supply chain location strategy
- Material specifications match local supply chain
- Fabrication methods are addressed in design

Optimized supply chain
- Electronic comp lifecycle analysis
- BoM part selection
- Lifecycle status
- Manufacture status
- Obsolescence risk
- RoHS compatible

Design for test – strategy
- Test strategy analysis
- Define test flow and access needs
- Consider product quality, volume, cost, end use, etc.

Design for test – schematic
- Schematic analysis

Design for assembly analysis
- Pre-place check
- BoM/CAD integrity
- Footprint check
- Post-place check
- Component spacing
- Edge clearances
- Fids/tooling holes

Design for test – access
- Prelim fan-out check

Design for manufacturability – process
- Pre-build check
- Assembly process
- Production build site

Design for test – strategy simulation
- Test strategy simulation
- Confirms "process test" flow
- Post PCB fabrication release (required input)

Design for manufacturability – feedback
- Post-build feedback
- Build experience
- Given by production build site
DFX EXCELLENCE FOCUS AREAS

- Global Environment
- Conceptual Design
- Initial Design
- Detailed Design
- Prototype Assembly
GLOBAL PRODUCT DESIGN ELEMENTS

Geographical differences

- Language
- Environmental (local/regional)
- Unit of measure (imperial versus metric)
- Identify controlling dimension
- Identify alternate dimension
- Verify accuracy of units
- Numerical reporting (decimal versus comma)
- Calendar (Gregorian versus Chinese versus Hebrew, etc.)
- Date reporting (dd/mm/yyyy, mm/dd/yyyy, yyyy/mm/dd)
- Work week (Monday-Friday or Sunday-Thursday)

Mars climate orbiter
GLOBAL MATERIAL SPECIFICATION

Some materials are controlled by global specifications

• Plastics
• Electronic components
• Printed circuit board laminates

Some materials are controlled by local/regional specifications

• Metals
• Finishes

4. MATERIAL IS AISI 1010-1020 COLD ROLLED STEEL OR APPROVED SUBSTITUTE
5. BREAK SHARP EDGES TO 0.25 MAXIMUM

4. MATERIAL IS SPCC, SECC, OR SAPH-440 STEEL
5. FINISH: ZINC PLATE PER ASTM 8633, TYPE 3, CLEAR OR YELLOW, SERVICE CONDITION 1. WIRE HUNG ONLY. DO NOT TUMBLE PLATE.

3. THIS IS A CAD DRAWING. DO NOT MANUALLY UPDATE
4. MATERIAL IS ALUMINUM ADC-10, ADC-12 OR ZINC ZDC2 OR APPROVED SUBSTITUTE. FINISH IS AS CAST
Component fabrication baseline processes can be different

Stamped metal fabrication
  • Sequential/progressive die system versus multiple single die machines (increased tolerance)

Plastic injection molding
  • Percentage of regrind/recycle material allowed

Machining
  • Metric versus imperial cutting tools (radius tolerance)
Global Environment

- Understand cultural differences
- Define default project conditions
- Address material variability in design
- Define component fabrication method
Physical design allocations

- Define X,Y-axis constrained design allocations for printed circuit board assembly and components
  - PCB/assembly size, feature and edge tolerances
  - Tight location tolerances for mechanical, electro-mechanical, opto-electronic components
  - Solder/adhesive position requirements

- Define Z-axis constrained design allocations for all elements
  - Components, PCB and component attachment (solder)
  - Other (insulators, covers, chassis, etc.)
Determines the optimal automated test strategy while balancing test costs versus overall yield and capacity for a particular PCB assembly and/or product

Uses available automated test technology

- Automated Optical Inspection (AOI)
- Automated X-ray Inspection (AXI)
- In-Circuit Test (ICT)
- Stand-alone boundary scan
- Flying probe
- Functional test
- Environmental

Multiple areas of analysis focus – select one or all

- Test routing (flow)
- Cost analysis
- Throughput analysis
- Line Replaceable Unit (LRU) analysis
- Printed circuit board assembly process test simulation
Component lifecycle analysis reduces the potential impact of near end-of-life components

RoHS/non-RoHS compatible analysis ensures compliance with regulatory and product reliability and assembly requirements

<table>
<thead>
<tr>
<th>Part #</th>
<th>Supplier</th>
<th>Lead-Free</th>
<th>RoHS</th>
<th>RoHS Exemption</th>
<th>RoHS Exemption Type</th>
<th>Component Engineer Comment</th>
<th>Terminal Plating</th>
<th>MSL</th>
<th>Max Temp</th>
<th>C of C/ Datasheet</th>
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<td>Kemet Electroics</td>
<td>Compliant</td>
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<td>No</td>
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<td>Link</td>
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<td>Compliant</td>
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<td>Link</td>
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<td>Compliant</td>
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High Risk
Completeness of bills of material (BoM)
• Correct procurable information
  - Manufacturer
  - Manufacturer’s part number
• Procurement quantity matches reference designator quantity

Alternate supplier packages
• All suppliers’ packages are equivalent
  - Functional
  - Length, width, height
  - Number of interconnections/leads
  - Packages match mounting pattern on printed circuit boards
Identifies circuit topologies that will interfere with the control and testing of components within an in-circuit test system

Review of the schematics for the following:
- Free-running oscillators
- Control pins tied hard to power or ground
- Control pins tied to a common net
- Asynchronous feedback loops
- Incorrect set-up of boundary scan devices
- No disable mechanism for batteries
- Missing access to pins – left as no-connects
COMPONENT PACKAGING AND DESIGN IMPACTS

Increased use of leadless component packaging technology
- Ball Grid Array (BGA)
- Quad Flatpack No-lead (QFN)

Increased sensitivity component/printed circuit board flatness
- Internal split plane or partial plane
- Nonfunctional pad removal

Increased use of component packaging with finer lead pitches
- 0.65mm > 0.5mm > 0.4mm > 0.35mm > 0.3mm > ?
• Define physical and functional constraints
• Define overall test strategy early
• Supply chain design is critical
• Application of test and component packaging
Placement and types of vias in pad can affect assembly solder joint formation

More of an impact on smaller components and/or lower number of electrical connections
Determines ability of a PCB fabricator to fabricate the PCB and/or issues that may affect cost and long-term reliability

Automated rules-driven checking process based on capabilities from a cross-section of multiple printed circuit board suppliers:

- Drill – micro-via, blind, buried, through-hole
- Plated through-hole annular ring
- Feature-to-feature clearance violations
- Feature size violations
- Silkscreen clearance and feature size
- Insufficient solder mask coverage or clearance
- Copper connectivity (netlist issues / net stubs)
- Fabrications panel utilization
Traditional G10 and FR4 printed circuit board laminates cannot survive multiple elevated lead free soldering process exposure or sustain impact to reliability.

Severity of reliability impacts are influenced by:
- Assembly process thermal exposure conditions
- Board design – number of layers, conductor routing
- Component package types
- Conductor / component placement density
- Operational environment

Photos courtesy of Cookson and Universal Instruments
Lead free laminate is less ductile
Lead free solder is less ductile
Increased stress transmission to internal connections
- Test fixture
- Assembly fixtures
- System integration
- Environmental
Increased PCB supplier control/capability understanding may be required to ensure proper etch compensation values are applied to other surface features and not to conductor patterns.

Percentage reduction by pad size

Supplier A

Supplier B
Non-solder mask defined (NSMD)
- Size of pad defined by copper pad and interconnections (variable size)
- Solder encapsulates pad
- Limited to components with lead pitch greater than 0.4mm

Solder mask defined (SMD)
- Size of pad defined by solder mask opening (uniform size)
- Solder covers exposed pad (fills opening)
- Required for components with lead pitch 0.4mm or less
- Preferred for leadless array devices like land grid arrays, multi-row quad flatpack no-leads, etc

Solder mask fabrication consistency
- Fabrication note interpretation “No solder mask permissible on pads unless provided this way on supplied artwork”
- Selective solder mask opening changes between PCB suppliers
Initial Design

- Use auto analysis to manage design technology
- Ensure delivered product matches design intent
- Understand lead-free implications and PCB fab constraints
- Note traditional tolerancing is inadequate
- Documentation ensures vendor implementation integrity
Analysis for issues that may affect the ability to assemble the PCB due to board outline, component, footprint, component placement and/or routing issues

Automated rules-driven checking based on DFX guidelines

- Bill of material analysis – BoM versus CAD
- Fiducial and tooling hole identification and analysis
- Component spacing analysis – body to body/edge etc.
- Component padstack analysis – pad to pad, pad to via, etc.
- Pin to pad/hole analysis
- Thermal connection analysis
- Solder paste stencil analysis
- Assembly panel utilization

Design database components are checked using independent like part definitions – simulate component placement
Verify design tool information matches physical dimensions of component package

- Component body – length, width, height
- Component pins match attachment pattern on printed circuit boards
  - Lead pitch to pad/hole pitch
  - Lead size to pad/hole size
  - Lead span to pad/hole size
  - Number of leads to pad/hole count
Number of layer connections to plated through-hole

- Increased number of layer connections increases thermal mass of plated through-hole
- Increased number of plane layer connections greatly increases thermal mass of plated through-hole
- Increase thermal pad isolation to improve solder flow to topside

Higher solder temperatures or increased solder dwell times create problems with pads on solder side
Components without leads are more sensitive to minor design and assembly process changes

- Land pattern design
  - Exposed pad size uniformity
- Component /printed circuit board flatness/warping
  - Copper distribution under package
- Paste volume control
  - Pad to pad volume
  - Pad to design defined volume
Multiple trace connections
  • Trace connections per pad
  • Uniformity across all pads on single component

Solder mask defined pad increased soldering defects
  • Delayed reflow across surface mount technology components
    - Tombstone components
    - “Ball in socket” area array component

“Via in pad” placement may create mounting pad height differences
  • More of an impact on smaller and/or lower lead count or leadless (no solder ball/solder bump) component packages
Determines probe accessibility to the various components/nets for the purpose of in-circuit testing

- Bottom and top side analysis – if required
- PCB design database component outlines will be substituted with validated component outline data per component manufacturer’s package information
- Rules based on design for test guidelines
  - Test point size
  - Test point to test point spacing
  - Component to test point spacing
  - Solder mask clearance
- Fixture induced printed circuit board bending strain estimate
Mechanical stress/strain impact analysis to identify test-initiated potential latent field failure modes

- Solder joint crack initiation or fracture
- Micro/buried via design impacts
  - Surface copper cracking/separation
  - Internal copper cracking/separation
- Mechanical strain concentration
  - Test point concentration
  - Final assembly/disassembly
Detailed Design

- Use auto analysis to manage complex design technology
- Verify accuracy of design tool to actual component data
- Incorporate assembly process into thermal design
- Note lead-free sensitivity to material finish differences
- Assess test accessibility and density
Smaller components decrease total PCB and assembly process tolerance

Minor misalignment can impact process yields

3 mil

6 mil
Stencil alignment of solder paste to pad tolerance may be critical to good manufacturing yields

(Dependant upon PCB surface finish)
Depending upon the pairing of PCB surface finish and component lead finish, the amount of solder wicking/spread can induce or reduce solder defect formation with lead free soldering process.
TO CLEAN OR NOT TO CLEAN?

Ability to remove soldering process residues from PCBs may change due to

- Component package type
- Component size
- Solder mask design
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Design for manufacturability – feedback
- Post-build feedback
- Build experience
- Given by production build site

Design for PCB fabrication analysis
- Pre-PCB fabrication check
- Netlist
- Drills
- Copper clearances
- Solder mask
- Silkscreen